MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023

ECP2046 – COMPUTER ORGANIZATION AND ARCHITECTURE

(TE, RE)

12 JULY 2023
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 3 pages excluding the cover page with 4 questions only.

2. Attempt ALL 4 questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the answer booklet provided.

QUESTION 1

a) Discuss and describe the signed magnitude representation. Give two weaknesses of this representation.

[2+2 marks]

b) Translate the following two complement numbers into their binary signed magnitude representation.

a. 1111 1011
b. 0000 1111

[2+2 marks]

c) Find the corresponding decimal number for the following IEEE-32-bit floating-point numbers with an 8-bit biased exponent.

i) 0 10000111 10000000000000000000000
ii) 1 01111010 00000000000000000000000

[5+5 marks]

d) Solve the following.

$$(-4 + 7) \times 3$$

Note:

- Represent the numbers using two's complement with the least number of bits
- Use two's complement addition and booth algorithm to solve the problem.
- Show the contents of each register for booth algorithm implementation

[7 marks]

Continued .....

QUESTION 2

a) Compare the indirect register addressing mode over the simple indirect addressing mode and comment on the instruction address field.

[2 marks]

b) State and discuss the three implementations of the displacement addressing mode. What is the pro and con of the displacement addressing mode?

[4 marks]

c) The registers in the processor can be broadly divided into two categories. Name these categories and elaborate on the general roles of the registers belonging to each of the categories.

[4 marks]

d) Name and discuss the branch prediction approaches that can be adapted to handle conditional branches.

[10 marks]

e) Given the initial values (in decimal) in the registers and assembly code as follows:
A=11, B=6, C=2, D=4, E=9

Instruction 1 (I1):	MOV X, A
Instruction 2 (I2):	ADD X, B
Instruction 3 (I3):	MOV Y, D
Instruction 4 (I4):	MUL Y, E
Instruction 5 (I5):	SUB Y, C
Instruction 6 (I6):	DIV Y, X

i) Determine the number of addresses of I4
ii) Determine the value of register X after I2 and before I3 in decimal
iii) Determine the value of register Y after I6 in decimal

[1+2+2 marks]

Continued .....

QUESTION 3

a) Draw a block diagram of a control unit.

[5 marks]

b) Following are the content of accumulator (AC), program counter (PC) register and memory location FFE0 at the beginning of a fetch cycle.

PC	FFE0
AC	0534

FFE0	0B83

Give all the microinstructions during the fetch cycle and illustrate the changes to all registers and memory locations involved.

[12 marks]

c) Discuss the principal of hardwired and microprogrammed control unit, highlight the advantages and disadvantages of each implementation.

[8 marks]

QUESTION 4

a) Intel 80486 which was introduced in 1989 used the x86 pipeline design.
   i) Discuss the pipeline stages of Intel 80486
   ii) Why there are two decode stages in the pipeline of Intel 80486?

[10+2 marks]

b) Identify and discuss the instruction hazards of superscalar architecture given the following sequence of instruction.

   i) MUL R6, R1, R2
      ADD R6, R4, R5
   ii) MUL R6, R1, R2
      ADD R7, R5, R6
   iii) DIV X3, X1, X2
      MUL X5, X4, X3
      ADD X4, X0, X6

[3+3+3 marks]

c) i) What is instruction issue policy?

[1 mark]

ii) State three types of instruction issue policies.

[3 marks]

End of Paper